HI-8400

Galvanically Isolated 4-Channel GND/Open or Supply/Open Sensor with Lightning Protection

July 2018

GENERAL DESCRIPTION

The HI-8400 is a galvanically isolated 4-channel discrete-to-digital sensor designed to output sensor data via a Serial Peripheral Interface (SPI) or parallel bus interface.

Galvanic isolation provides 800V isolation between each of the sensors and the logic interface. This is an ideal device for systems that must tolerate different grounds.

Each input is individually pin configurable as either GND/Open or Supply/Open (28V/Open). Discrete input thresholds are compliant to the Airbus ABD0100H and MIL-STD-704 specification.

The part operates from a 3.3V (+/-5%) or 5.0V (+/-5%) digital supply and 28V analog supply for each isolated sensor.

A 1mA wetting current is sourced from the input network on each SENSE input when GND/Open mode is selected for that pin. The wetting current serves to prevent dry relay or switch contacts. A sensor output interrupt pin alerts the system to a change in sensor input, avoiding constant polling via SPI to check status.

All sense inputs are internally lightning protected to RTCA/DO160G, Section 22 Level 3 Pin Injection Test Waveform Set A (3 & 4), Set B (3 & 5A) and Set Z (3 & 5B) with respect to the sensor return ground, without using external components.

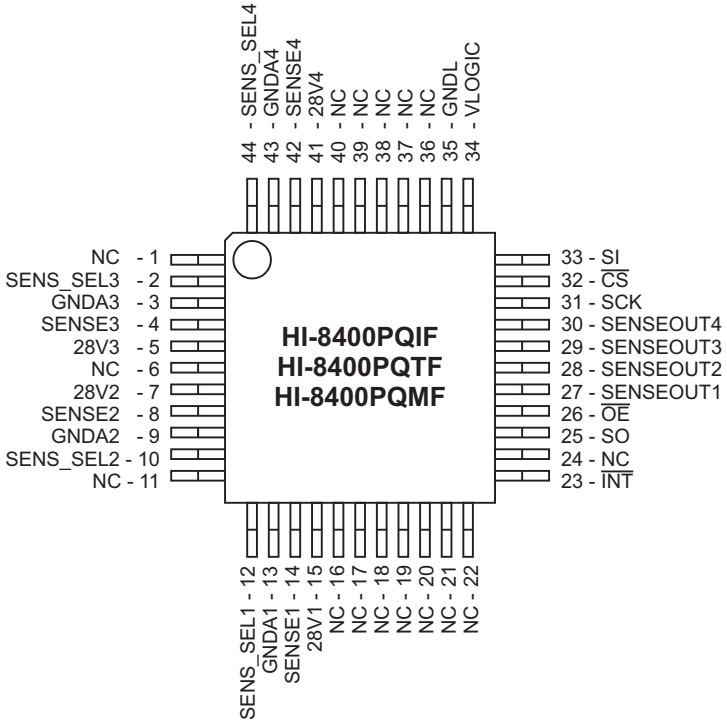
APPLICATION

- Avionics Discrete to Digital Sensing in systems that must tolerate different grounds or require Galvanic Isolation for fault isolation.

FEATURES

- Airbus ABD0100H and MIL-STD-704 standard compliant sensor thresholds
- Galvanically isolated discrete-to-digital sensor providing 800V isolation between each sensor and the logic interface
- Four discrete inputs, individually pin configurable as GND/Open or Supply/Open
- Sensor data outputs read through SPI or parallel bus
- Sense inputs lightning protected to RTCA/DO1060G, Section 22, Level 3
- 5MHz Serial Peripheral Interface (SPI) allows daisy-chaining of parts for efficient board routing
- Interrupt generated on any change of sensor state
- Withstands inadvertent application of 115V AC/400Hz power to sense inputs.

PIN CONFIGURATION



44 - Pin Plastic Quad Flat Pack (PQFP)

BLOCK DIAGRAM

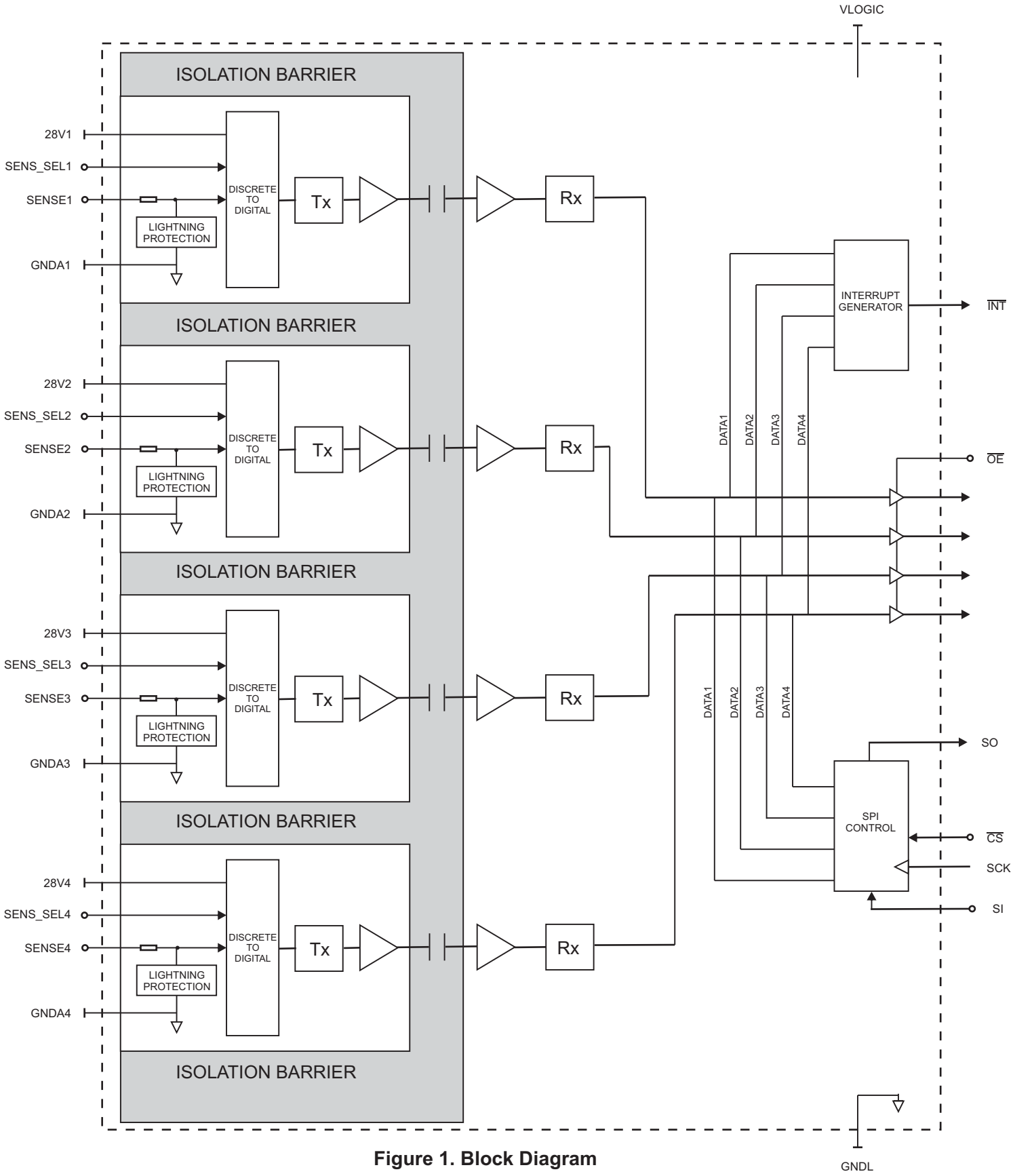


Figure 1. Block Diagram

PIN DESCRIPTIONS

PIN	SYMBOL	FUNCTION	DESCRIPTION
1	NC		No Connect
2	SENS_SEL3	Discrete Input	Sensor 3 configuration definition (GNDA3 = GND/Open; 28V3 = Supply/Open). 540kΩ Pull-down
3	GNDA3	Supply	Sensor Ground 3
4	SENSE3	Discrete Input	Sense input 3. Mapped to the third SPI bit shifted out of SO during data read
5	28V3	Supply	28V supply voltage Sensor 3
6	NC		No Connect
7	28V2	Supply	28V supply voltage Sensor 2
8	SENSE2	Discrete Input	Sense input 2. Mapped to the second SPI bit shifted out of SO during data read
9	GNDA2	Supply	Sensor Ground 2
10	SENS_SEL2	Discrete Input	Sensor 2 configuration definition (GNDA2 = GND/Open; 28V2 = Supply/Open). 540kΩ Pull-down
11	NC		No Connect
12	SENSE_SEL1	Discrete Input	Sensor 1 configuration definition (GNDA1 = GND/Open; 28V1 = Supply/Open). 540kΩ Pull-down
13	GNDA1	Supply	Sensor Ground 1
14	SENSE1	Discrete Input	Sense input 1. Mapped to the first SPI bit shifted out of SO during data read
15	28V1	Supply	28V supply voltage Sensor 1
16	NC		No Connect
17	NC		No Connect
18	NC		No Connect
19	NC		No Connect
20	NC		No Connect
21	NC		No Connect
22	NC		No Connect
23	$\overline{INT}$	Digital Output	Interrupt output, generates 1us low pulse when any sensor changes state, open drain
24	NC		No Connect
25	SO	Digital Output	SPI data output
26	$\overline{OE}$	Logic Input	Strobe for parallel bus
27	SENSEOUT1	Logic Output	Parallel Sensor Output 1
28	SENSEOUT2	Logic Output	Parallel Sensor Output 2
29	SENSEOUT3	Logic Output	Parallel Sensor Output 3
30	SENSEOUT4	Logic Output	Parallel Sensor Output 4
31	SCK	Logic Input	SPI clock input. (10MHz maximum clock frequency at 5V or 5MHz at 3.3V)
32	$\overline{CS}$	Logic Input	Chip select. SPI data transfers are enabled when $\overline{CS}$ is low
33	SI	Logic Input	SPI data input for daisy chain applications
34	Vlogic	Supply	Logic Supply Voltage
35	GNDL	Supply	Logic Ground
36	NC		No Connect
37	NC		No Connect
38	NC		No Connect
39	NC		No Connect
40	NC		No Connect
41	28V4	Supply	28V supply voltage Sensor 4
42	SENSE4	Discrete Input	Sense input 4. Mapped to the forth SPI bit shifted out of SO during data read
43	GNDA4	Supply	Sensor Ground 4
44	SENS_SEL4	Discrete Input	Sensor 4 configuration definition (GNDA4 = GND/Open; 28V4 = Supply/Open). 540kΩ Pull-down

FUNCTIONAL DESCRIPTION

OVERVIEW

The HI-8400 is comprised of 4 sensors, which may be individually pin configured for GND/Open or Supply/Open (also known as 28V/Open) sensing. SENS_SEL pins are used to set the sensor configuration. If Low (grounded or floating), SENSE pins are sensing GND/Open. If High, SENSE pins are sensing Supply/Open.

An open drain interrupt pin ($\overline{INT}$) generates a 1µs low pulse when any of the sensor outputs change state. This eliminates the need for the micro-contoller to poll the data register at frequent intervals.

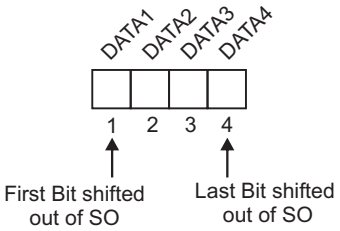
Thresholds are as defined in the Airbus ABD0100H standard based on the sensor configuration in either GND/Open or Supply/Open mode. Reading the data register is accomplished using a serial interface compatible with the industry-standard Serial Peripheral Interface (SPI) bus or parallel SENSE output pins.

Figure 1 shows a simplified block diagram of the HI-8400.

DATA REGISTER

A four-bit Data Register captures the output state from the four discrete sensors. Data is latched on the falling edge of $\overline{CS}$. The Data bits are read out from the chip over the serial interface. Sensor 1 data bit is output first at SO followed by the remaining three sensor states. In either mode (GND/Open or Supply/Open), a logic one is output when the voltage at the sensor pin input is greater than the high threshold and a logic zero is output when the sensor voltage is lower than the low threshold.

Multiple HI-8400s may be daisy-chained together to allow a single SPI sequence to capture data from several ICs in one operation.



SUPPLY/OPEN SENSING

To program as Supply/Open sensors, SENS_SELn (where n is the sensor number) is tied to the 28Vn supply pin.

Open and Supply or 28V states are detected according to the threshold levels VSLO and VSHI . When the SENSE input exceeds VSHI, the output of the sensor goes high, indicating 28V state. The output of the sensor remains high until a voltage of less than VSLO is detected at the SENSE input, representing an Open state and causing the sensor output to go low. The Sensor will maintain an Open detect state until the SENSE input becomes greater than VSHI. The difference VSHI - VSLO represents the hysteresis which improves noise immunity and reduces output chattering.

WETTING CURRENT

For the Supply/Open case the wetting current into the sense input is simply the current sunk by an effective 30 kΩ to GND. For V_{SENSE} = 28V, I_{WET} is about 1 mA.

GND/OPEN SENSING

To program GND/Open sensing, the SENS_SELn (where n is the sensor number) is tied to the GNDAn supply pin.

Open and Closed states are detected according to the threshold levels VGLO and VGHI . When the SENSE input exceeds VGHI, the output of the sensor goes high, indicating Open state. The output of the sensor remains high until a voltage of less than VGLO is detected at the SENSE input, representing a valid Ground state and causing the sensor output to go low. The Sensor will maintain a Ground detect state until the SENSE input becomes greater than VGHI. The difference VGHI - VGLO represents the hysteresis which improves noise immunity and reduces output chattering.

WETTING CURRENT

In GND/Open mode a current is sourced from the SENSE pin when it is grounded and 28Vn is powered. This current, called the “wetting current”, serves to provide current through switches or relay contacts to prevent dry contacts and improve switch contact reliability. The wetting current in this configuration is about 1mA.

FUNCTIONAL DESCRIPTION (cont.)

SERIAL PERIPHERAL INTERFACE

The HI-8400 uses a SPI (Serial Peripheral Interface) for host access to the Data Register which stores sensor status. Host serial communication is enabled through the active low, Chip Select ($\overline{CS}$) pin, and is accessed via a four-wire interface consisting of Serial Data Input (SI) from the host, Serial Data Output (SO) to the host, the Serial Clock (SCK) and the $\overline{CS}$. All read cycles are completely self-timed.

The SPI protocol specifies master and slave operation; the HI-8400 operates as a SPI slave.

The SPI protocol defines two parameters, CPOL (clock polarity) and CPHA (clock phase). The possible CPOL-CPHA combinations define four possible “SPI Modes”. The HI-8400 operation is based on Mode 0 (CPHA = 0, CPOL = 0), where input data for each device is clocked on the rising edge of SCK, and output data for each device changes on the falling edge of SCK. The host SPI logic must be configured for mode 0. SPI Mode 0 holds SCK in the low state when idle.

The SPI bus transfers serial data in multiples of 4 bits, depending on the number of devices (daisy chain application possible). Once $\overline{CS}$ is asserted, the rising edge of SCK shifts the input data into the slave devices. A rising edge on $\overline{CS}$ completes the serial transfer and re-initializes the HI-8400 SPI for the next transfer (see Figure 2).

Both master and slave simultaneously send and receive serial data (full duplex), per Figure 2. The HI-8400 maintains high impedance on the SO output whenever $\overline{CS}$ is high. The maximum SCK frequency is 5MHz at 3.3V or 10MHz at 5.0V. The HI-8400 logic is fully static and therefore there is no minimum SCK speed.

DATA REGISTER SPI TRANSFERS

When $\overline{CS}$ goes low, the output of each sensor is latched into the Data Register and SD1 is output at SO. The next 3 falling edges of SCK shift out Data Register bits SD2 through SD4. Simultaneously, data presented at SI is shifted into the Data Register. See Figure 2.

As seen in Figure 3, this data transfer method allows multiple HI-8400 devices to be “daisy-chained” such that the Data Registers from each device are cascaded to form a single shift register. Figure 4 shows a typical configuration of three daisy-chained HI-8400s to form a 12-input sensor array. Note that when reading from more than one device, $\overline{CS}$ must remain low throughout the data read sequence. Taking $\overline{CS}$ high and then low again between four-bit reads will cause the sensor data to be re-latched into the Data Registers, overwriting data shifted in from earlier HI-8400s in the chain.

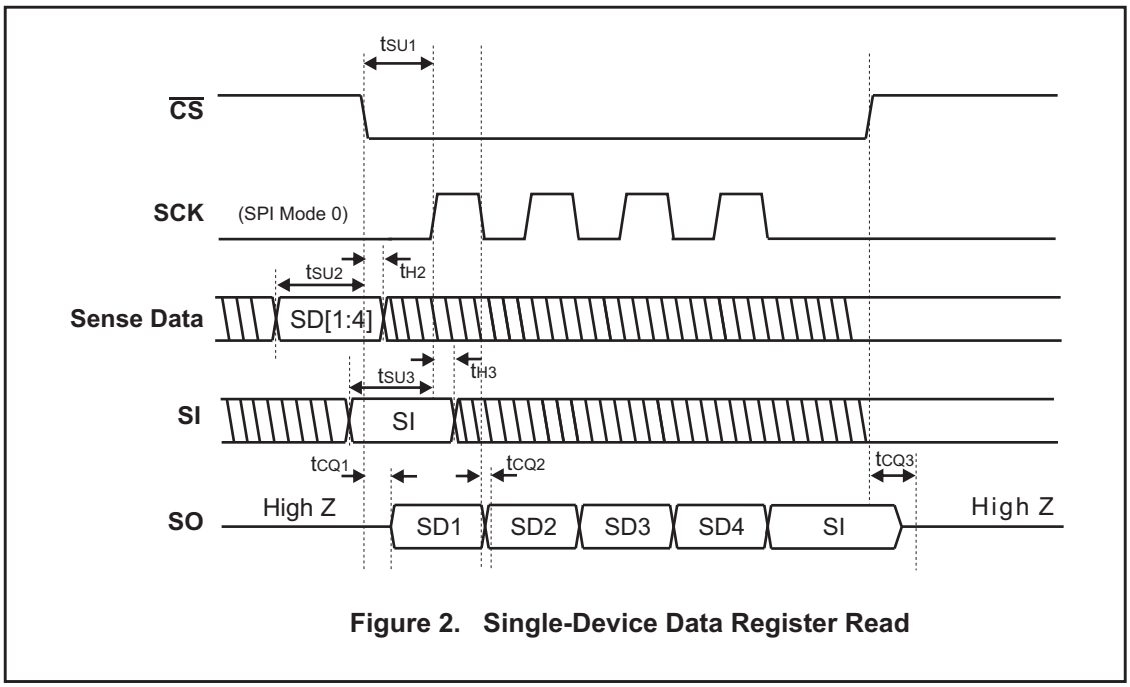


Figure 2. Single-Device Data Register Read

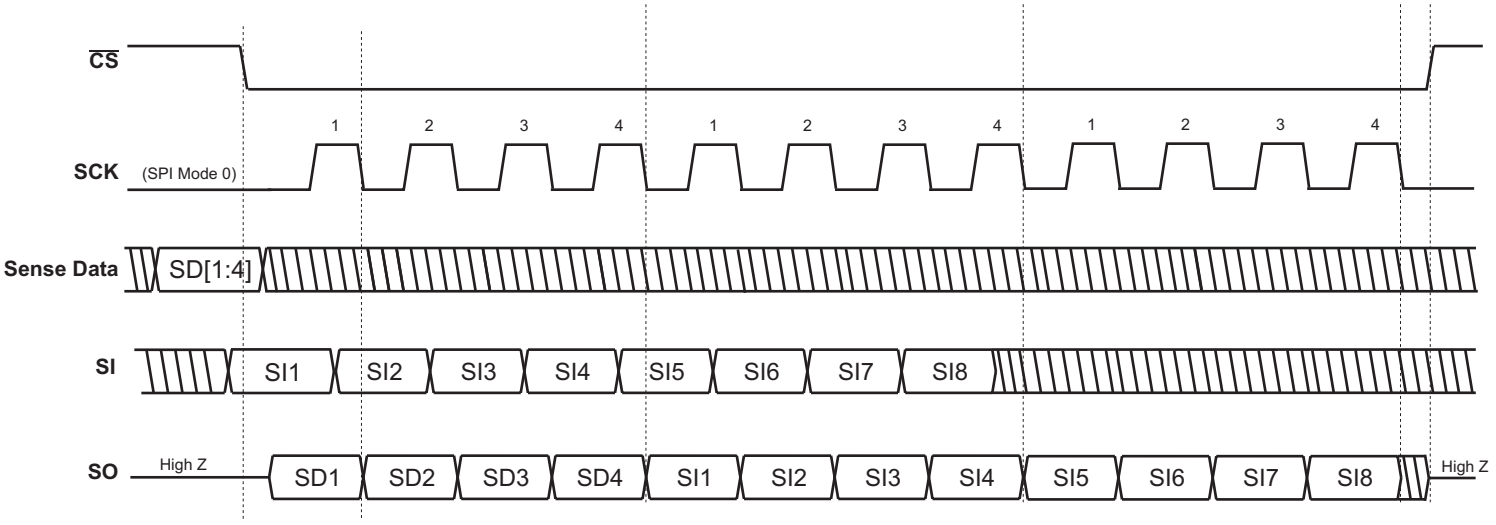


Figure 3. Three-Device SPI Daisy-Chain Data Register Read Example

FUNCTIONAL DESCRIPTION (cont.)

INTERRUPT FUNCTION

The $\overline{INT}$ output will generate 1µs low pulse when any sensor changes state. If multiple sensors change state within 1µs, the HI-8400 will OR all of the detected changes, and the pulse duration will increase accordingly.

24 Channel Sensor Application using HI-8400

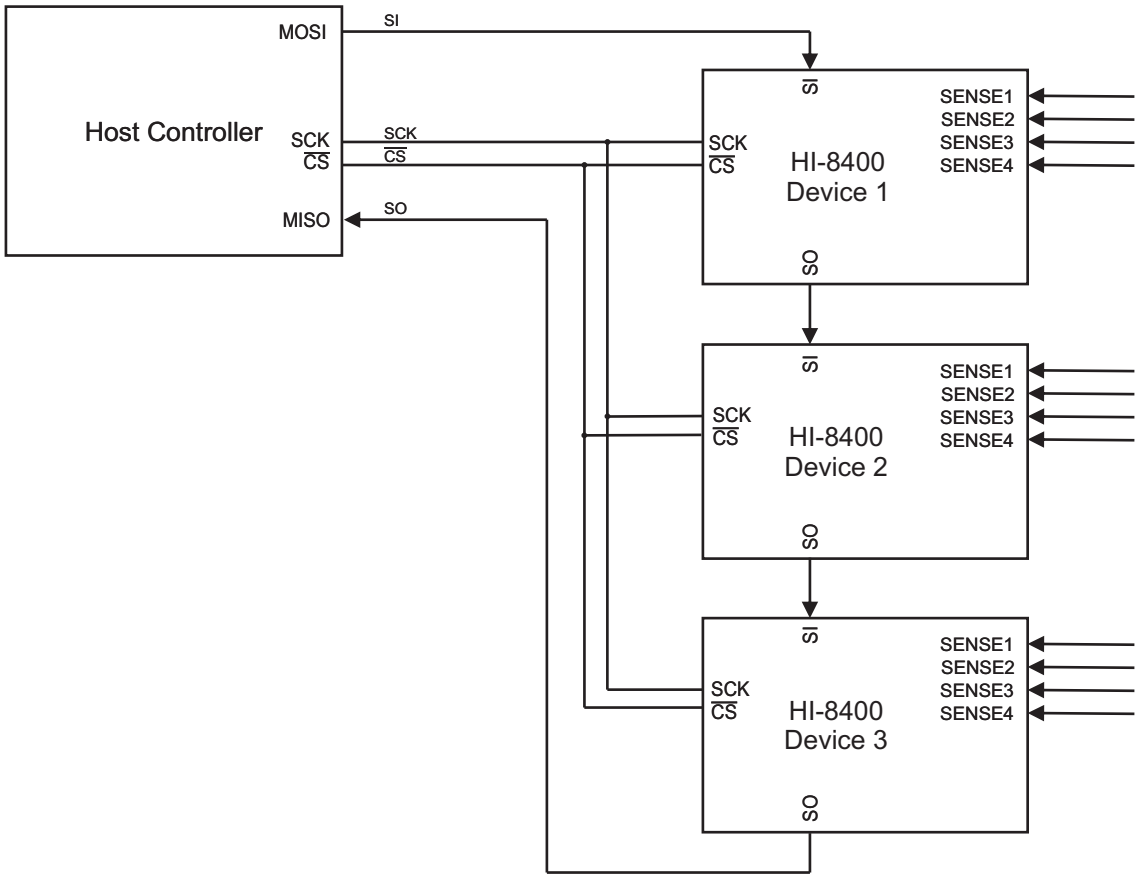


Figure 4. Multiple Chip "Daisy-Chain" Connection

FUNCTIONAL DESCRIPTION (cont.)

LIGHTNING PROTECTION

All SENSEn inputs are protected to RTCA/DO-160G, Section 22, Categories A3 and B3, Waveforms 3, 4, 5A, 5B with no external components with respect to the sensor return ground. Table 1 and Figure 5 give values and waveforms. Higher levels of lightning protection can be implemented using a series resistor and a TVS, see Application Note AN-305 for recommendations.

Level	Waveforms			
	3/3	4/1	5A/5A	5B/5B
	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)	Voc (V) / Isc (A)
3	600/24	300/60	300/300	300/300

Table 1. Waveform Peak Amplitudes

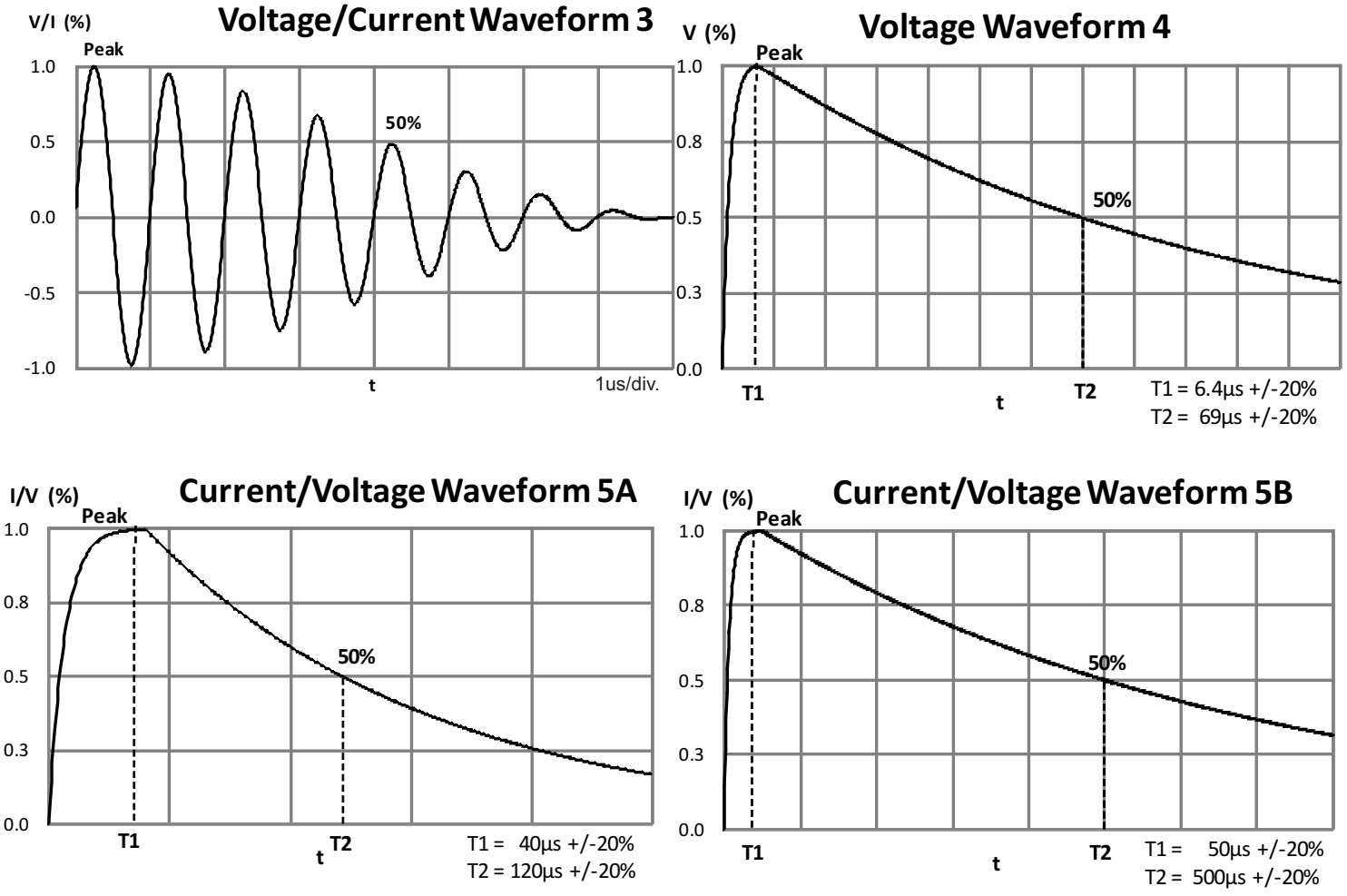


Figure 5. Lightning Waveforms

ABSOLUTE MAXIMUM RATINGS

Digital Supply Voltage (V_{LOGIC} wrt GNDL) ..... -0.3 V to +7V
Analog Supply Voltage (28Vn wrt GNDAn) ..... -0.3 V to +50V
Logic Input Voltage Range (wrt to GNDL) ..... -0.3V to V_{LOGIC} + 0.3V
Common-Mode Sensor Input Voltage (referenced to GNDL) (DC) ..... -800V to +800V
Discrete Input Voltage Range (referenced to GNDAn) (DC) ..... -80V to +80V (AC, 60 - 400Hz) 115Vrms
Continuous Power Dissipation (TA=+125°C) 1.7W
Solder Temperature (reflow) ..... 260°C
Junction Temperature ..... 175°C
Storage Temperature ..... -65°C to -150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

V_{LOGIC}	3.3V or 5.0V (+/- 10%)
28Vn	17V to 36V
Digital Inputs	0 to V_{LOGIC}
SENSE inputs	-4.0V to 49V
SENSE_SEL	0V to 28Vn

Operating Temperature Range

Industrial Screening	-40°C to +85°C
Hi-Temp Screening	-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

D.C. ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.0V to 5.5V, V_{DD} = 17.0V to 36.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
SENSE Inputs, Configured as Ground / Open (internal pull-up).						
OPEN state input voltage range	V_{GHIR}		10.5		49	V
Input threshold voltage HI	V_{GHI}		9.0		10.5	V
High level input current	I_{GHI}	V_{GHI} = 28V, 28Vn = 28V V_{GHI} = 49V, 28Vn = 28V		17 45	100 250	µA uA
GND state input voltage range	V_{GLOR}		-4		4.5	V
Input threshold voltage LO	V_{GLO}		4.5		6.0	V
Low level input current	I_{GLO}	V_{SENSE} = 0V, 28Vn = 28V	-0.5	-1.0	-1.5	mA
Input hysteresis voltage	V_{GHYS}	V_{GHI} - V_{GLO}	3.0			V
Input Floating Voltage	V_{FLOAT}	Sense inputs floating, not driven	2V + V_{GHI}			V
SENSE Inputs, Configured as Supply / Open (internal pull-down).						
Supply (28V) state input voltage range	V_{SHIR}		12.0		49	V
Input threshold voltage HI	V_{SHI}		10.5		12.0	V
High level input current	I_{SHI}	V_{SHI} = 28V, 28Vn = 28V	0.45	0.9	1.35	mA
OPEN state input voltage range	V_{SLOR}		-4.0		6.0	V
Input threshold voltage LO	V_{SLO}		6.0		7.5	V
Input hysteresis voltage	V_{SHYS}	V_{SHI} - V_{SLO}	3.0			V
Power Supply						
Logic supply current	I_{LOGIC}	V_{IN} = V_{LOGIC} or Ground, SENSE pins open		1.8	3.0	mA
Analog supply current (total, all sensors)	I_{DD}	V_{IN} = V_{LOGIC} or Ground SENSE pins open SENSE pins = Ground		 15 23	 24 33	 mA mA
Interrupt						
Current	Iout		300		550	uA
Logic Inputs / Outputs						
High level input voltage	V_{IH}	V_{LOGIC} = 3.0 to 5.5V	2.0			V
Low level input voltage	V_{IL}	V_{LOGIC} = 3.0 to 5.5V			0.8	V
Input hysteresis voltage, SCK input	V_{CHYS}	Note 1.	50			mV
High level output voltage	V_{OH}	I_{OUT} = -20 µA I_{OUT} = -4 mA, V_{LOGIC} = 3.0V	V_{LOGIC} -0.1 2.4			V V
Low level output voltage	V_{OL}	I_{OUT} = 20 µA I_{OUT} = 4 mA, VLOGIC = 3.0V			0.1 0.4	V V
Input leakage current	I_{IN}	V_{IN} = V_{LOGIC} or Ground	-10		+10	µA
Tri-state leakage current, SO output	I_{OZ}	V_{OUT} = V_{LOGIC} or Ground	-10		+10	µA

Note 1. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS

V_{LOGIC} = 3.0V to 5.5V, V_{DD} = 17.0V to 36V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYM	CONDITION	MIN	TYP	MAX	UNIT
3V Supply Domain						
SCK Frequency	f_{MAX}	50% Duty Cycle	0.1		5	MHz
CSN negedge to SCLK posedge	t_{SU1}		100			ns
Sensor Data Valid to CSN negedge	t_{SU2}		3			µs
Sensor Data Hold to CSN negedge	t_{HU2}		10			ns
SI Valid to SCLK posedge	t_{SU3}		25			ns
SI Hold to SCLK posedge	t_{H3}		10			ns
CSN nedgedge to SO	t_{CQ1}				45	ns
SCLK negedge to SO	t_{CQ2}				45	ns
CSN negedge to SO	t_{CQ3}				45	ns
Sensor input change to parallel output valid	t_{PROP}				5	µs
Min. Sense Input Pulsewidth	t_{SD}		3			µs
5V Supply Domain						
SCK Frequency	f_{MAX}	50% Duty Cycle	0.1		10	MHz
CSN negedge to SCLK posedge	t_{SU1}		50			ns
Sensor Data Valid to CSN negedge	t_{SU2}		7			µs
Sensor Data Hold to CSN negedge	t_{HU2}		5			ns
SI Valid to SCLK posedge	t_{SU3}		15			ns
SI Hold to SCLK posedge	t_{H3}		5			ns
CSN nedgedge to SO	t_{CQ1}				30	ns
SCLK negedge to SO	t_{CQ2}				30	ns
CSN negedge to SO	t_{CQ3}				30	ns
Sensor input change to parallel output valid	t_{PROP}				10	µs
Min. Sense Input Pulsewidth	t_{SD}		7			µs
Interrupt						
$\overline{INT}$ Pulse Width	INT			1		µs

ORDERING INFORMATION

HI - 8400PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn /Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PQ	44-lead Quad Flat Pack QFP

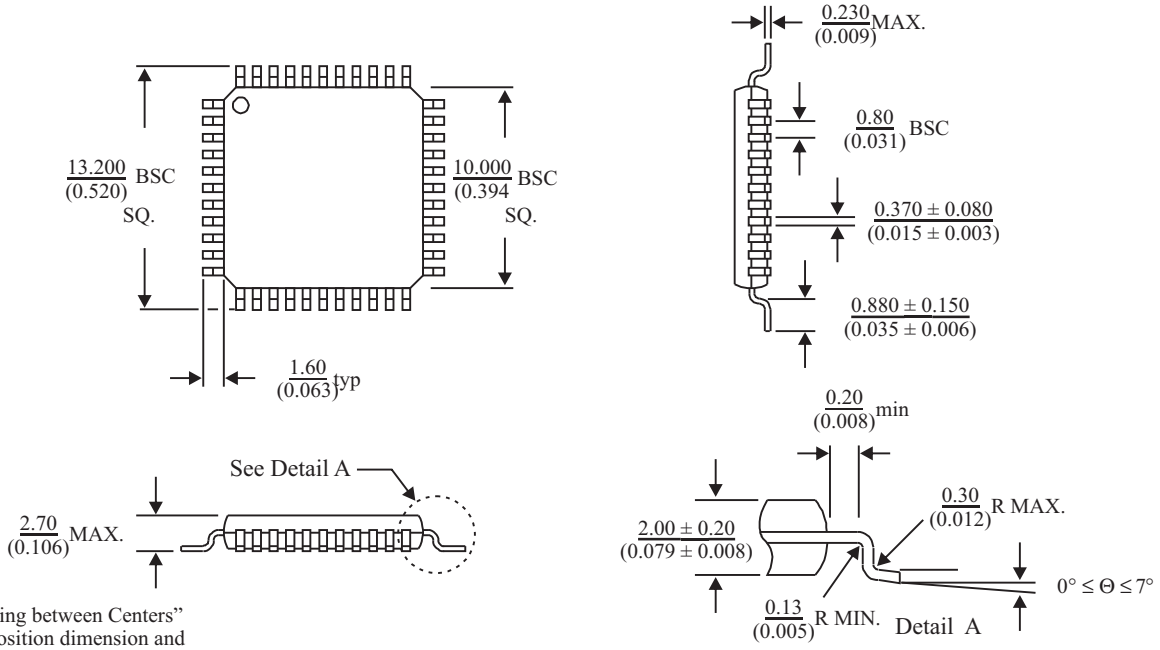
REVISION HISTORY

P/N	Rev	Date	Description of Change
DS8400	Prelim.	07/25/18	Initial Release.

44-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 44PMQS



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)