ADK-5200
Quick Start Guide:

HI-5200 10Base-T/100Base-TX
Physical Layer Transceiver

April 2018

REVISION HISTORY

Revision	Date	Description of Change
QSG-5200, Rev. New	02-09-18	Initial Release
Rev. A	04-23-18	Remove HI-5201 option

Introduction

The Holt HI-5200 is a 10Base-T/100Base-TX physical layer transceiver with both MII and RMII MAC interfaces. It utilizes a unique mixed-signal design to extend signaling distance while reducing power consumption, and offers HP Auto MDI/MDI-X for reliable detection of and correction for crossover and straight-through cables. The device comes in a 32-pin, lead-free QFN package and provides an ideal solution for 10Base-T/100Base-TX applications that have limited PCB board space.

The HI-5200 ADK evaluation board, ADK-5200, provides a convenient platform to evaluate HI-5200 features. All device configuration pins are accessible either by jumpers, test points or interface connectors on the board.

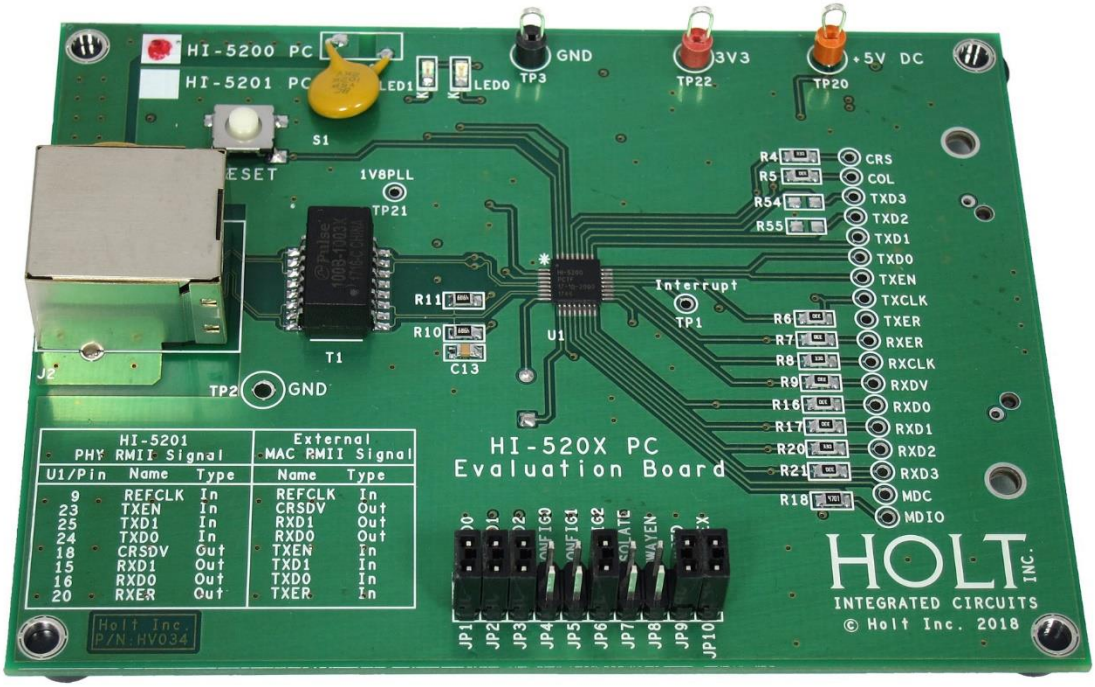


Figure 1. HI-5200 ADK Evaluation Board, ADK-5200

Features

- Holt 10Base-T/100Base-TX Physical Layer Transceiver
- RJ-45 Jack for Fast Ethernet cable interface
- HP Auto-MDIX for automatic detection and correction for straight-through and crossover cables
- MII (Media Independent Interface) connector to interface with a MAC controller
- RMII (Reduced MII) option with external 50MHz system clock
- 2 LED Indicators for status and activity
- Jumpers to configure strapping pins
- Manual Reset Button for quick reboot after re-configuration of strapping pins

Hardware Design Overview

Figure 2 shows a block diagram of the HI-5200 ADK evaluation board. It plugs into any industry standard "Fast Ethernet" board with Ethernet MACs that expose the MII interface. Configuration of the HI-5200 is accomplished through on-board jumper selections and/or by PHY register access via the MDC/MDIO management pins of the MII Interface.

Other features include a RJ-45 Jack for "Fast Ethernet" cable connection, programmable LEDs for reporting link status and activity, and a manual reset button for quick reboot after reconfiguration of strapping pins.

The HI-5200 evaluation board receives +5V DC input power through its MII connector.

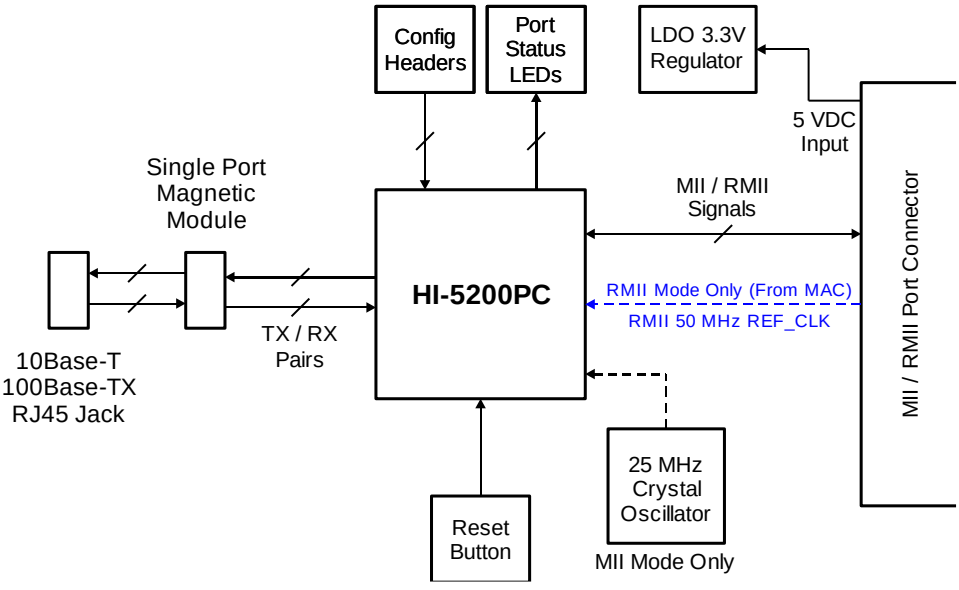


Figure 2. ADK-5200 Evaluation Board Block Diagram

MII (Media Independent Interface) Default Configuration

The MII interface is defined by Clause 22 of the IEEE 802.3 Specification. The HI-5200 PHY evaluation board receives power and accesses MII data and management information from the MII connector J1. In MII mode, the PHY is clocked at 25 MHz. A crystal oscillator on the board provides the clock, or an external 25MHz clock can be connected to the XI pin.

MII Management (MIIM) is conducted thru pins MDC (clock line) and MDIO (data line). MIIM allows upper-layer devices to monitor and control the states of the HI-5200. An external device with MDC/MDIO capability can read the PHY status or configure/write the PHY registers. The MIIM frame format and timing information can be found in the HI-5200 Datasheet and in Clause 22 of the IEEE 802.3 Specification.

The HI-5200 PHY board has a bottom-side 50-pin connector J1 for MII connection. Table 1 lists the pin-outs for the MII interface on connector J1.

Table 1. Connector J1 Fast Ethernet Port MII Pin Definition.

J1 Pin #	Signal		J1 Pin #	Signal
1	--		2	--
3	--		4	--
5	+5V		6	+5V
7	MDIO		8	GND
9	MDC		10	GND
11	RXD3		12	GND
13	RXS2		14	GND
15	RXD1		16	GND
17	RXD0		18	GND
19	RXDV		20	GND
21	RXCLK		22	GND
23	RXER		24	GND
25	TXER		26	GND
27	TXCLK		28	GND

J1 Pin #	Signal		J1 Pin #	Signal
29	TXEN		30	GND
31	TXD0		32	GND
33	TXD1		34	GND
35	TXD2		36	GND
37	TXD3		38	GND
39	COL		40	GND
41	CRS		42	GND
43	+5V		44	+5V
45	--		46	--
47	--		48	--
49	--		50	--

RMII (Reduced Media Independent Interface) Configuration Option

The HI-5200 ADK PHY evaluation board can use its 50-pin male edge connector (J1) with some minor board population changes to interface with RMII MACs. Like MII mode, the HI-5200 ADK PHY evaluation board, ADK-5200, receives power and accesses RMII data and management information via connector J1 in RMII mode. In RMII mode, the 50MHz clock (from the MAC) is connected to the XI pin.

The HI-5200 ADK PHY evaluation board and MAC hardware devices can be configured to RMII mode and interface with each other using the same J1 connector interface. The board changes to support RMII mode are as follows:

1. Remove crystal circuit (Y1, C16, C17) and TXC clock termination (R6).
2. Populate R14 with 0 Ohm and R19 with 33 Ohm to connect HI-5200 RMII 50MHz reference clock (provided by MAC side via J1 pin 27) to U1 pin 9 (XI input).
3. Select RMII mode by setting strapping pins CONFIG[2:0] to ‘001’.

These board changes can also be found in the HI-5200 ADK PHY evaluation board schematic diagram.

Table 2 lists the pin outs for the RMII interface on connector J1.

Table 2. Connector J1 Fast Ethernet Port RMII Pin Definition.

J1 Pin #	Signal		J1 Pin #	Signal
1	--		2	--
3	--		4	--
5	+5V		6	+5V
7	MDIO		8	GND
9	MDC		10	GND
11	not used		12	GND
13	not used		14	GND
15	RXD1		16	GND
17	RXD0		18	GND
19	RXDV		20	GND
21	not used		22	GND
23	RXER		24	GND
25	not used		26	GND
27	REFCLK		28	GND
29	TXEN		30	GND
31	TXD0		32	GND
33	TXD1		34	GND
35	not used		36	GND
37	not used		38	GND
39	not used		40	GND
41	not used		42	GND

J1 Pin #	Signal		J1 Pin #	Signal
43	+5V		44	+5V
45	--		46	--
47	--		48	--
49	--		50	--

Jumper Setting & Definition

The HI-5200 ADK PHY evaluation board does not require any jumper for normal operation. At power-up, the HI-5200 ADK PHY is configured using the chip's internal pull-up and pull-down resistors with its default strapping pin values. Jumpers are provided to override the default settings, allowing for quick configuration and re-configuration of the board. To override the default settings, simply select and close the desired jumper setting(s) and toggle the on-board manual reset button (S1) for the new setting(s) to take effect.

The HI-5200 ADK PHY evaluation board jumper settings are defined in Table 3 below.

Table 3. HI-5200PC Evaluation Board Jumper Definitions.

Jumper	**Definition**	**Open (default)**	**Closed**
JP1	PHYAD0	1	0
JP2	PHYAD1	0	1
JP3	PHYAD2	0	1
Jumper	**Definition**	**CONFIG[2:0]**	**Mode**
JP4	CONFIG0	[open, open, open]	MII (default)
JP5	CONFIG1	[open, open, close]	RMII
JP6	CONFIG2	[close, open, open]	PCS Loopback
All other CONFIG[2:0] combinations are reserved, not used.			
Jumper	**Definition**	**Open (default)**	**Closed**
JP7	Isolate Mode	Disabled	Enabled
JP8	Auto Negotiation	Enabled	Disabled
JP9	Forced Speed	100Base-TX	10Base-T
JP10	Forced Duplex	Half Duplex	Full Duplex

Table 4 lists the pin strapping definitions for the HI-5200 ADK PHY evaluation board jumpers.

Table 4. HI-5200PC Pin Strapping Options on PHY Evaluation Board.

Jumper	U1 Pin #	Pin Name	Pin Function
JP3 JP2 JP1	15 14 13	PHYAD2 PHYAD1 PHYAD0	The PHY address is latched at power-up / reset and is configurable to any value from 1 to 7. The default PHY address is 00001. PHY address bits [4:3] are always set to 00.
JP6 JP5 JP4	18 29 28	CONFIG2 CONFIG1 CONFIG0	The CONFIG[2:0] pins are latched at power-up / reset and are defined as follows: CONFIG[2:0] = 000 MII Mode (default) CONFIG[2:0] = 001 RMII Mode CONFIG[2:0] = 100 PCS Loopback All other CONFIG[2:0] combinations are reserved.
JP7	20	ISO	ISOLATE Mode Pull-Up = Enable Pull-Down = Disable (default) At power-up / reset, the state of this pin is latched into register 0 bit 10.
JP9	31	SPEED	SPEED Mode Pull-Up = 100Mbps (default) Pull-Down = 10Mbps At power-up / reset, the state of this pin is latched into register 0 bit 13 as the Speed Select, and is also latched into register 4 (Auto Negotiation Advertisement) as the Speed capability support.
JP10	16	DUPLEX	DUPLEX Mode Pull-Up = Half Duplex (default) Pull-Down = Full Duplex At power-up / reset, the state of this pin is latched into register 0 bit 8 as the Duplex Mode.
JP8	30	NWAYEN	Nway Auto-Negotiation Enable Pull-Up = Enable Auto-Negotiation (default) Pull-Down = Disable Auto-Negotiation At power-up / reset, the state of this pin is latched into register 0 bit 12.

Test Point Definition

The HI-5200 ADK PHY evaluation board has six test points. They are defined in the following table.

Table 5. HI-5200PC PHY Evaluation Board Test Points.

Test Point	Description
TP1	Interrupt Signal (U1 pin 21) with external pull-up
TP2	Signal Ground
TP3	Signal Ground
TP20	+5VDC input DC voltage check
TP21	+1.8VDC core logic PLL voltage check
TP22	+3.3VDC IC supply voltage check

RJ-45 Ethernet Connector

The RJ-45 Connector (J2) connects to standard CAT-5 Ethernet cable to interface with 10Base-T/100Base-TX Ethernet devices.

J2 also supports Auto-MDIX and Auto-Negotiation / Forced Modes.

LED Indicators

The board has two LED indicators (LED0 and LED1). LED1 is connected to pin 31 and LED0 is connected to pin 30 of the HI-5200PC (U1),

The two LEDs are programmable to LED mode '00' or '01' via register 1E (hex), bits [15:14], and are defined in the following table.

Table 6. Definitions for HI-5200PC PHY Evaluation Board LEDs.

LED Mode	**LED1 (U1 pin 31)**			**LED0 (U1 pin 30)**		
00	**Speed**	**U1 Pin 31 State**	**LED State**	**Link / Activity**	**U1 Pin 30 State**	**LED State**
	10BT	H	OFF	No Link	H	OFF
	100BT	L	ON	Link	L	ON
	----------	----------	----------	Activity	Toggle	Blinking
01	**Activity**	**U1 Pin 31 State**	**LED State**	**Link**	**U1 Pin 30 State**	**LED State**
	No Activity	H	OFF	No Link	H	OFF
	Activity	L	ON	Link	L	ON
10	Reserved – Not Used			Reserved – Not Used		
11	Reserved – Not Used			Reserved – Not Used		

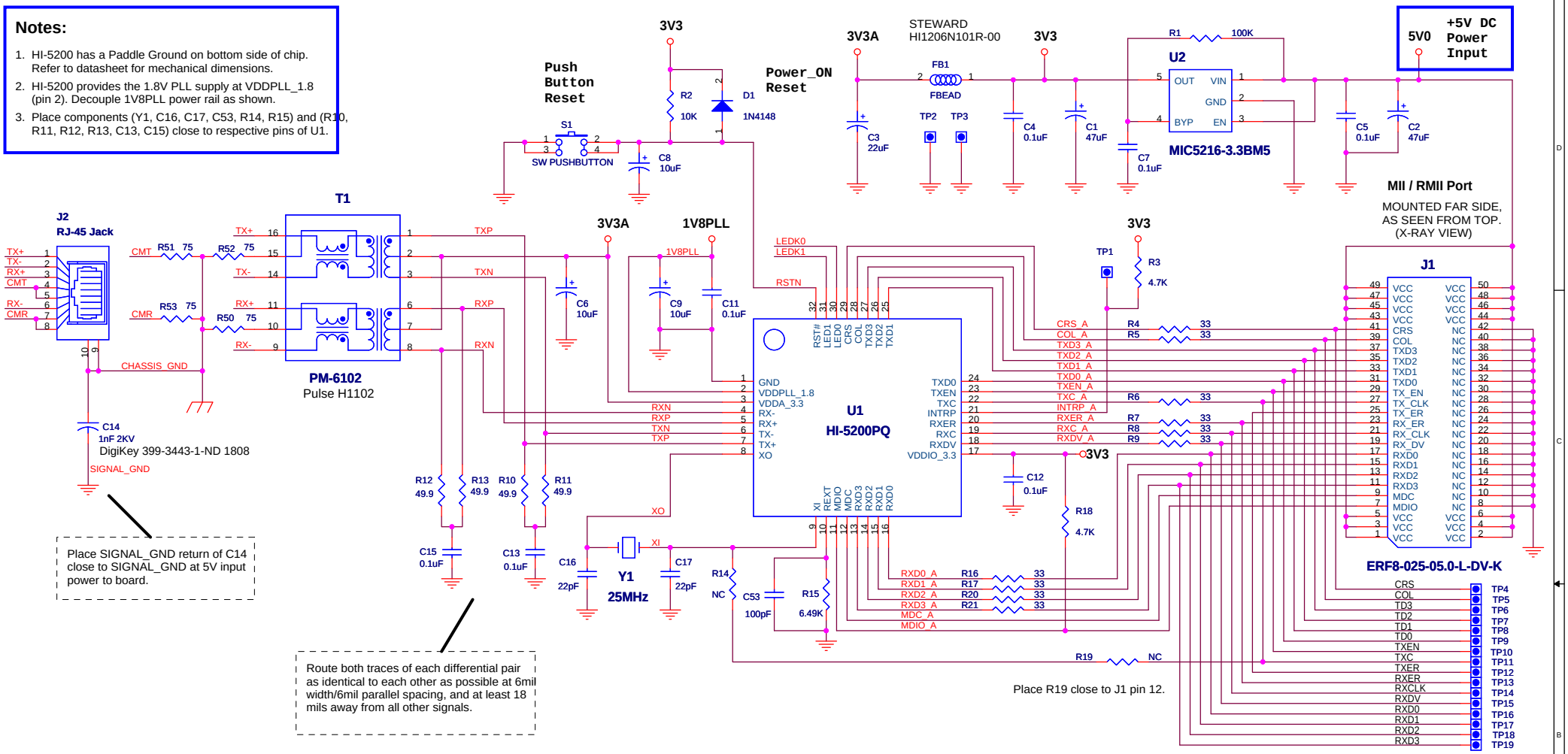
PCB Rev. A
P/N: HV032

Bill of Materials
HI-520X PC PQ
Evaluation Board

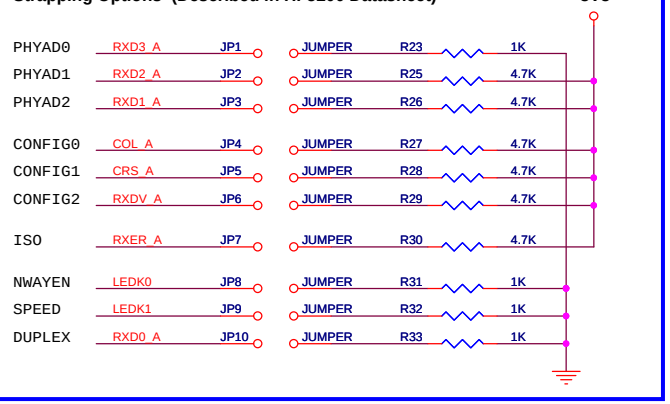
Item	Qty	Description	Reference	Digikey P/N	Mfg P/N
1	1	PCB, Bare, Evaluation Board	N/A		JetTech # 42169
2	7	Capacitor Cer 0.1uF 25V 10% X7R 0805	C4,C5,C7,C11, C12,C13,C15	399-1168-1-ND	Kemet C0805C104K3RACTU
3	2	Capacitor Cer 22pF 50V COG 0805 SMD	C16,C17	399-1113-1-ND	Kemet C0805C220J5GACTU
4	1	Capacitor Cer 100pF 50V COG 0805 SMD	C19	399-1122-1-ND	Kemet C0805C101J5GACTU
5	2	Capacitor Cer 1000pF, 2KV Y5P Radial	C14,C18	1252PH-ND	Vishay S102K33Y5PP63K5R
6	1	Capacitor Cer 10uF 16V X5R 0805 SMD	C8	399-8013-1-ND	Kemet C0805C106M4PACTU
7	2	Capacitor Tant 10uF 16V 10% 6032 SMD	C6,C9	399-3732-1-ND	Kemet T491C106K016AT
8	1	Capacitor Tant 22uF 16V 10% 6032 SMD	C3	399-3744-1-ND	Kemet T491C226K016AT
9	2	Capacitor Tant 47uF 16V 20% 6032	C1,C2	399-8356-1-ND	Kemet T491C476K016AT
10	2	Resistor 0, 1/8W 5% 0805 SMD	R54,R55 Optional	P0.0ACT-ND	Panasonic ERJ-6GEY0R00V
11	10	Resistor 33, 1/8W 5% 0805 SMD	R4-R9,R16,R17,R20,R21	P33ACT-ND	Panasonic ERJ-6GEYJ330V
12	4	Resistor 49.9, 1/8W 1% 0805 SMD	R10-R13	P49.9CCT-ND	Panasonic ERJ-6ENF49R9V
13	4	Resistor 75, 1/8W 5% 0805 SMD	R50,R51,R52,R53	P75ACT-ND	Panasonic ERJ-6GEYJ750V
14	2	Resistor 220, 1/8W 5% 0805 SMD	R22,R24	P220ACT-ND	Panasonic ERJ-6GEYJ221V
15	4	Resistor 1K, 1/8W 5% 0805 SMD	R23,R31,R32,R33,	P1.0KACT-ND	Panasonic ERJ-6GEYJ102V
16	8	Resistor 4.7K,1/8W 5% 0805 SMD	R3,R18,R25-R30,	P4.7KACT-ND	Panasonic ERJ-6GEYJ472V
17	1	Resistor 6.49K, 1/8W 1% 0805 SMD	R15	P6.49KCCT-ND	Panasonic ERJ-6ENF6491V
18	2	Resistor 10K, 1/8W 5% 0805 SMD	R1,R2	P10KACT-ND	Panasonic ERJ-6GEYJ103V
19	1	Diode Gen 100V 300mA SOD 123	D1	1N4148W-FDICT-ND	Diode Inc. 1N4148W-7-F
20	1	Ferrite Bead 31 Ohm 1206 SMD	FB1	445-6170-1-ND	TDK HF50ACB321611-T
21	2	Test Point, Black Insulator, 0.062"	GND (TP2, TP3)	36-5011-ND	Keystone 5011
22	1	Test Point, Red Insulator, 0.062"	3V3 (TP22)	36-5010-ND	Keystone 5012
23	1	Test Point, Orange Insulator, 0.062"	5V (TP20)	36-5013-ND	Keystone 5013
24	1	LED Green 0805 SMD	LED1	160-1423-1-ND	LiteOn LTST-C171GKT
25	1	LED Red 0805 SMD	LED2	160-1178-1-ND	LiteOn LTST-C171EKT
26	1	Header, Male 2x20, .1" Pitch	JP1-JP10	S2012EC-20-ND	Sullins PREC020DAAN-RC
27	10	Conn Shunt Gold	JP1-JP10	S9001-ND	Sullins SPC02SYAN
28	1	Switch Tactile SPST-No 0.02A, 15V	S1	P19749CT-ND	Panasonic EVP-BFAC1A000
29	1	Socket, 50 pin .8mm Edge Assembly	J1	ERF8-025-05.0-L-DV-K	Samtec ERF8-025-05.0-L-DV-K
30	1	Con Mod 8P8C R/A Shield RJ45	J2	AE10387-ND	Assman A-2004-2-4-LPS-N-R
31	1	10/100Base-T 1:1 Single Port 16Term, Gull SMD	T1	100B-1003X	Arrow Pulse 100B-1003X
32	1	Crystal 25Mhz 18pF Leaded HC49/US	Y1	XC1927-ND	ECS-250-18-4X-DU
33	1	IC Reg Linear 3.3V 500mA SOT23-5	U2	576-2756-1-ND	Micro Chip MIC5216-3.3YM5-TR
34	1	HI-520X PQ & PC	U1	Holt Inc.	HI-520X PQ & PC
35	4	Bumper Cylin 0.312" Dia, 0.210" High, Blk	Place at four corners	SJ5747-0-ND	3M SJ61A11

Notes:

1. HI-5200 has a Paddle Ground on bottom side of chip. Refer to datasheet for mechanical dimensions.
2. HI-5200 provides the 1.8V PLL supply at VDDPLL_1.8 (pin 2). Decouple 1V8PLL power rail as shown.
3. Place components (Y1, C16, C17, C53, R14, R15) and (R10, R11, R12, R13, C13, C15) close to respective pins of U1.



Strapping Options (Described in HI-5200 Datasheet)



RMII Mode (option)

The RMII signal connections between HI-5200 PHY and external MAC are shown in the table to the right.

For RMII mode,

1. Remove crystal circuit (Y1, C16, C17) and TXC termination (R6).

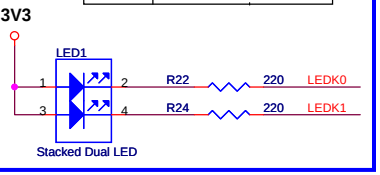
2. Populate R14 with 0 Ohm and R19 with 33 Ohms to connect 50MHz Reference Clock (provided by the MAC side via J1 pin 27) to U1 pin 9 (XI input).

3. Select RMII mode by setting jumpers JP6:JP4 for signals CONFIG[2:0] to '001'.

4. Connect J2 (RMII Port) to board with RMII MAC .

HI-5200 PHY RMII Signals			External MAC RMII Signals	
Name	U1 Pin	Type	Name	Type
REFCLK	9	Input	REF_CLK	Output
TX_EN	23	Input	CRS_DV	Output
TXD[1]	25	Input	RXD[1]	Output
TXD[0]	24	Input	RXD[0]	Output
CRSDV	18	Output	TX_EN	Input
RXD[1]	15	Output	TXD[1]	Input
RXD[0]	16	Output	TXD[0]	Input
RX_ER	20	Output	TX_ER	Input

LED Mode	[00]	[01]
LED0	LINK/ACT	LINK
LED1	SPEED	ACT



HOLT INTEGRATED CIRCUITS

Title: HI-5200PQ Evaluation Board

Size | Document Number: 5200_EVAL.DSN | Rev: B

Date: Monday, April 23, 2018 | Sheet 1 of 1