MIL-STD-1553/1760 Protocol IP Core

HI-6300

Product Brief

Features

- Software compatible with Holt's existing hardware solutions: MAMBA™ or HI-6130/31 families
- BC/RT/MT or RT/MT variants
- IP is based on fully validated IC solution
- Available DO-254 Certification Package supporting Design Assurance Level A
- Up to 64K words static RAM with RAM Error Detection/Correction option.
- Concurrent multi-terminal operation
- Synchronous AXI Host Interface
- Built-in self-test feature
- Fully programmable Bus Controller with 28 op code instruction set
- Independent time-tag counters for all terminals with 32-bit option for Bus Controller and 48-bit option for Monitor Terminal
- Simple Monitor Terminal (SMT) records commands and data separately, with 16-bit or 48-bit time tag
- 32-deep Interrupt buffer
- MIL-STD-1760 Boot mode to initialize RT with Busy Bit set without host intervention

Benefits

- Holt is a well-established supplier of the MIL-STD-1553 physical layer
- Short lead times – Always in stock!

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General Description

The Holt MIL-STD-1553 / MIL-STD-1760 IP core solution provides a complete and compliant single or multi-function interface between a host processor and MIL-STD-1553B bus. The IP Core supports Bus Controller (BC), Monitor Terminal (MT) or Remote Terminal (RT) functions, with all options having a high-performance synchronous host interface, allowing easy connection to AMBA AXI4 interface protocol or PCI-Express. Enabled terminals communicate with the MIL-STD-1553 buses through a shared dual bus transceiver, HI-1587, and external isolation transformer, also available from Holt.

The HI-6300 is the only MIL-STD-1553 IP Core providing native Error Detection and Correction on the embedded 8K or 64K words of block RAM. The user-provided input clock is selectable from 50 or 100MHz. A comprehensive built-in self-test is also available and MIL-STD-1760 busy bit response time is supported with an external input signal.

The Holt Multi-Core IP product includes a Verilog IP core, test bench, and supporting documentation, allowing designers to instantiate the core in a variety of FPGA or ASIC implementations. Also available is a high-level API software library supporting Linux, VxWorks, or bare metal implementations. The API is compatible with competitor legacy APIs allowing developers to reuse existing application software.

Bus Controller

The Bus Controller (BC) is programmed using a set of 28 instruction op codes, greatly reducing the host's processing workload. It can optionally use a 16 or a 32-bit time base, clocked from a choice of six internally generated clocks, or an external time base clock. Special BC op codes manage all 32-bit time base functions.

The programmable Bus Controller autonomously supports multi-frame message scheduling, message retry schemes, storage of message data, asynchronous message insertion and status/error reporting to the host processor.

Monitor Terminal

Bus Monitor Terminal (MT) functionality passively records MIL-STD-1553 bus activity. Message commands, terminal responses and message data are stored in internal RAM. The SMT records commands and data separately and can utilize 16 or 48-bit time tags with a range of clocking options.

Remote Terminal

The RT is software compatible with Holt's popular MAMBA™ and HI-6130/31 Remote Terminals, which have been fully validated. RAM buffer options include single, double and 2 circular buffer choices.

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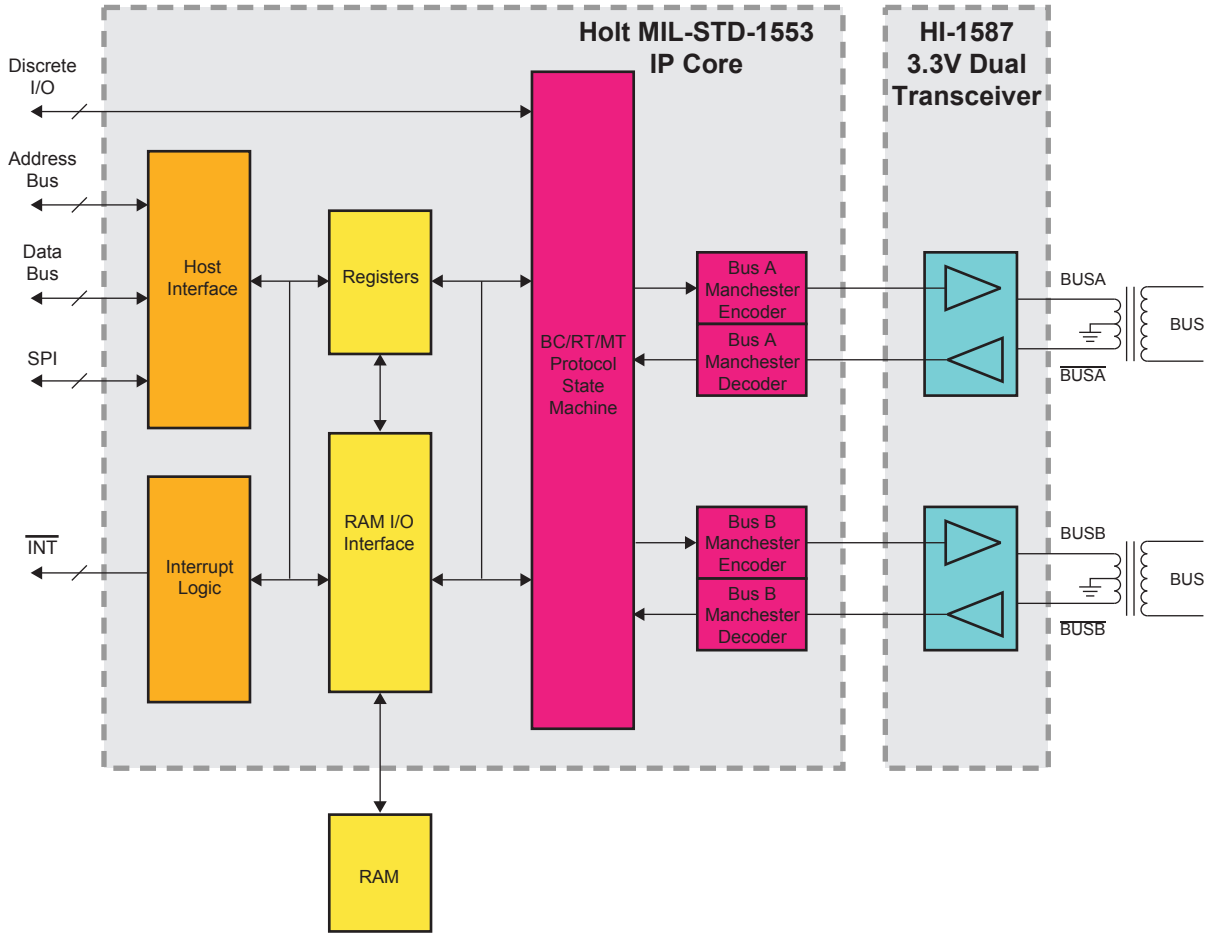

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