HI-2130: Protocol, RAM, dual transceivers and dual transformers in a single package
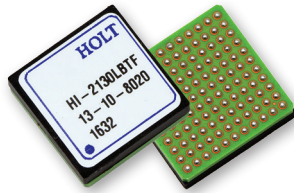
Features

- Smallest footprint MIL-STD-1553/MIL-STD-1760 solution available (includes transformers)
- Combined functionality of HI-6130 and HI-6131 in a single package with integrated transformers
- Low profile package solution (4.4mm) suitable for PMC and XMC applications
- Hermetically sealed die option (MSL1) available
- Extended temperature range, -55ºC to +125ºC
- Less expensive than traditional multi-chip modules
- DO-254 certifiable
- Concurrent multi-terminal operation (BC, MT, 1 or 2 independent RTs)
- 64K bytes on-chip RAM with error detection/correction option
- Two host interface options in one package: 16-bit parallel or SPI
- Fully programmable Bus Controller with 28 op code instruction set
- Independent time-tag counters for all terminals with 32-bit option for Bus Controller and 48-bit option for Monitor Terminal
- Simple Monitor Terminal (SMT) Mode records commands and data separately, with 16-bit or 48-bit time tagging
- IRIG Monitor Terminal (IMT) Mode supports IRIG-106 Chapter 10 packet format. Complete IRIG-106 data packets including full packet headers and trailers can optionally be generated
- Interrupt log buffer with hardware-assisted interrupt decoding records the most recent 32 interrupts
- Built-in self-test for protocol logic, digital signal paths and internal RAM
- Optional self-initialization using external EEPROM
- Two temperature ranges: -40ºC to +85ºC, or -55ºC to +125ºC
- Short lead times – Always in stock!

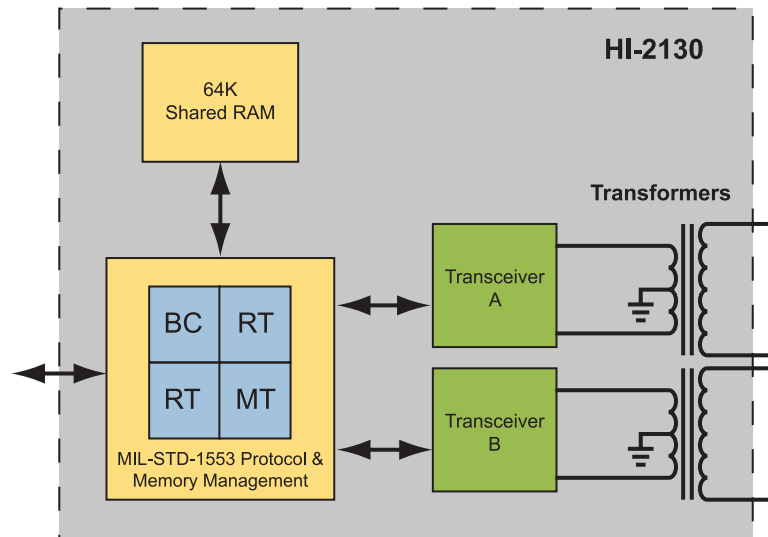*For further information on these and other Holt products contact:*

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ISO 9001:2008 Registered

Bus Controller

The BC is a programmable message-sequencing device for control in MIL-STD-1553B applications. Programmed using a set of 28 instruction op codes, the BC greatly reduces the host's processing workload. The BC can optionally use a 16- or a 32-bit time base, clocked from a choice of six internally generated clocks, or an external time base clock. Special BC op codes manage all 32-bit time base functions.

The programmable Bus Controller autonomously supports multi-frame message scheduling, message retry schemes, storage of message data, asynchronous message insertion and status /error reporting to the host processor.

Monitor Terminal

The Bus Monitor Terminal (MT) passively records MIL-STD-1553 bus activity. Message commands, terminal responses and message data are stored in internal RAM, using one of two possible modes. Simple Monitor Terminal (SMT) and IRIG Monitor Terminal (IMT) Modes are targeted for different applications. When operating in SMT mode, the MT records commands and data separately. The SMT can utilize 16- or 48-bit time tags with a range of clocking options.
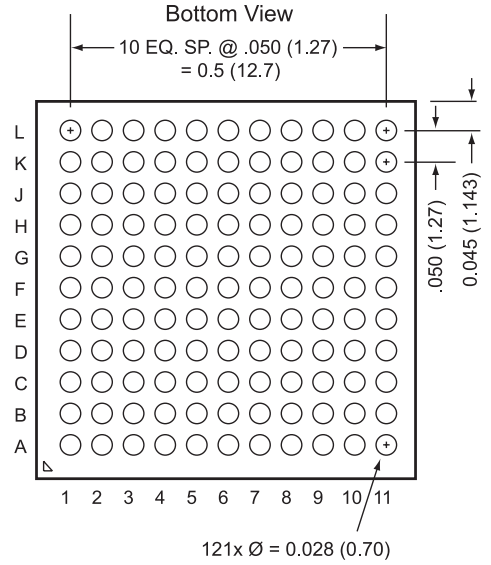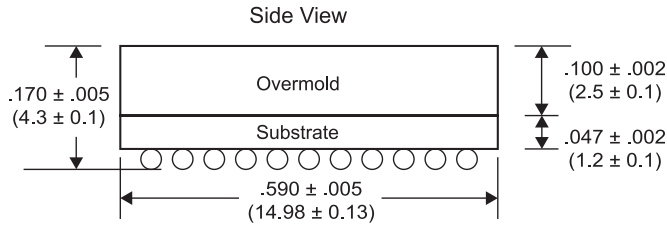
The IMT mode operation is designed to meet data recording requirements of Telemetry Standard RCC Document 106-07, Chapter 10. This "IRIG 106 Chapter 10" data recorder uses 48-bit relative time stamping, having 10MHz (100ns) resolution. Message time stamps occur at one of three selectable message progress points. Several error handling schemes are available. Bus Monitor interrupts notify the host when stack rollover occurs, or when a user-programmed stack level has been reached. The IMT stores message records in the assigned stack using IRIG 106 "packet body" format. The device can optionally generate complete IRIG 106 packets, including full packet headers and trailers meeting IRIG 106 Chapter 10 requirements.

Remote Terminals

The device is configurable to operate as one or two Remote Terminals. The RTs are modeled after the popular Holt HI-6130/31 Remote Terminal and have been fully validated. The two Remote Terminals operate with independent characteristics, each RT having fully separate RAM structures (e.g., descriptor and illegal command tables) and independent configuration and status registers. RAM buffer options include single, double and 2 circular buffer choices. The two RTs can be reset and re-initialized independently. The full benefit of two autonomous RTs is achieved while using the same complexity and circuit board area as a single Remote Terminal.

Ball Grid Array (121BGA3)

Side View

Overmold

Substrate

.170 ± .005
(4.3 ± 0.1)

.100 ± .002
(2.5 ± 0.1)

.047 ± .002
(1.2 ± 0.1)

.590 ± .005
(14.98 ± 0.13)

Bottom View

10 EQ. SP. @ .050 (1.27)
= 0.5 (12.7)

.050 (1.27)

0.045 (1.143)

L K J H G F E D C B A

1 2 3 4 5 6 7 8 9 10 11

121x Ø = 0.028 (0.70)

Dimensions in inches (millimeters)

Block diagram — HI-2130 containing HI-6130 / HI-6131

Discrete Signal Outputs: IRQ, MTPKRDY, READY, ACTIVE, RT1MC8, RT2MC8

64K Static RAM and Registers

Host Interface: BWID, BTYPE, WPOL, WE, RE, A0, WAIT, A15:1, D15:0, BUS / SPI, CE, SCK, MOSI, MISO

Memory and Register Access Control — Address, Data, Control

BC Message Processor
MT Message Processor
RT1 Message Processor
RT2 Message Processor

Tx 1553 Words / Rx 1553 Words

Bus A Manchester Encoder
Bus A Manchester Decoder
Bus B Manchester Encoder
Bus B Manchester Decoder

Configuration Option Logic: RT1A4 - 0, RT1AP, RT2A4 - 0, RT2AP, BENDI, RT1LOCK, RT2LOCK, MTSTOFF, RAMEDC

INTERNAL CLOCKS: MCLK, TTCLK, MTTCLK

TXINHA
BUSA
BUSA

TXINHB
BUSB
BUSB

Reset & Initialization Logic: AUTOEN, EECOPY, MR

Discrete Signal Inputs: BCENA, BCTRIG, MTRUN, RT1ENA, RT2ENA, ACKIRQ, RT1SSF, RT2SSF

Serial Peripheral Interface (SPI) to EEPROM

Test Logic: TEST, MODE

POWER: GND, VDD

ESCK, ECS, MISO, MOSI

OPTIONAL SERIAL EEPROM (AUTO-CONFIG)

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