

Overview

The purpose of this notification is to announce that Holt Integrated Circuits has made a Die Revision Change to the HI-6110 Product which will result in a change to its data sheet.

Description

Holt Integrated Circuits is implementing two design changes to improve product robustness in metal layers one and two. The first design change will disable GAPERR (gap error) in BC mode. Error Register bit 4 will be held low for BC mode. Deactivation of this error flag does not affect assertion of the ERROR output signal for other error-causing conditions. This change has no effect on RT, MT or MT-RT modes of operation.

The second change corrects false error assertion for certain conditions when monitoring RT-to-RT messages in Bus Monitor (MT) mode, with or without assigned RT address. This design change has no effect on BC or RT mode.

This improvement will result in a die revision change for the HI-6110 product from Revision M to Revision N and a data sheet change from Revision K to Revision L.

The PCN Change type is to Function only (Design). There is no change to Fit, Form, Quality or Reliability.

Reason

The first design change eliminates false error assertion following successful completion of BC-to-RT receive commands. The second design change corrects an error which was falsely asserted when the terminal address for one party in an RT-RT message matched an RT address from a specific, previous message transaction.

Products Affected

Table 1 summarizes the products affected by this PCN. All parts listed are affected by this change. This includes devices in both the standard and Pb-free packages and devices in all grades; industrial, high temperature and military.

Table 1: Products Affected

6110PQI	6110PQT	6110PQM	6110PCI	6110PCT	6110PCM
6110PQIF	6110PQTF	6110PQMF	6110PCIF	6110PCTF	6110PCMF

Traceability

A Date Code and Country of Origin facilitate package traceability. Parts from Table 1 will be shipped starting from Jun 14, 2008 (Date Code: 0823 & Country of Origin: Malaysia) and after.

Qualification Data

Reliability Test	Requirement	Comment
Device Characterization	Final Test yield analysis over -55°C and +125°C temperature extremes.	No reliability qualification test is required as a result of this change

Response

Note: In accordance with JESD46-C, this change is deemed accepted by the customer if no acknowledgement is received within 30 days from this notice.

No response is required. For additional information or questions, please contact:

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Additional Documentation

Below is a list of documents that are associated with this notice:

- DS6110 Rev. L (Eliminate references to the BC Mode GAPERR bit in the Error Register description, on page 7)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision Description
5/14/08	1.0	Initial Release